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| **Course Number** | ELE 734 |
| **Course Title** | Low-Power Digital Integrated Circuits |
| **Semester/Year** | F2020 |
| **Lab No** | 04 |
| **Instructor Name** | Dr. Andy Ye |
| **Section No** | 06 |

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| **Submission Date** | 12/07/2020 |
| **Due Date** | 12/07/2020 |

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| **Name** | **Student ID** | **Signature\*** |
| Vatsal Shreekant | 500771363 |  |

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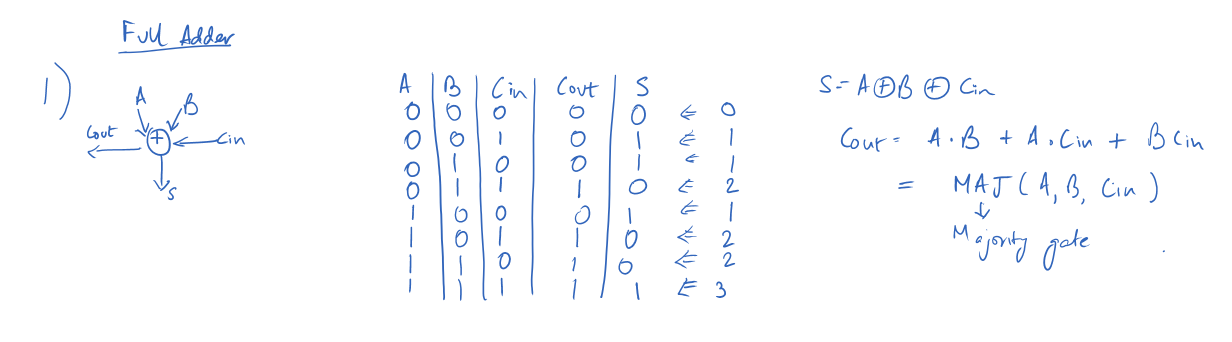
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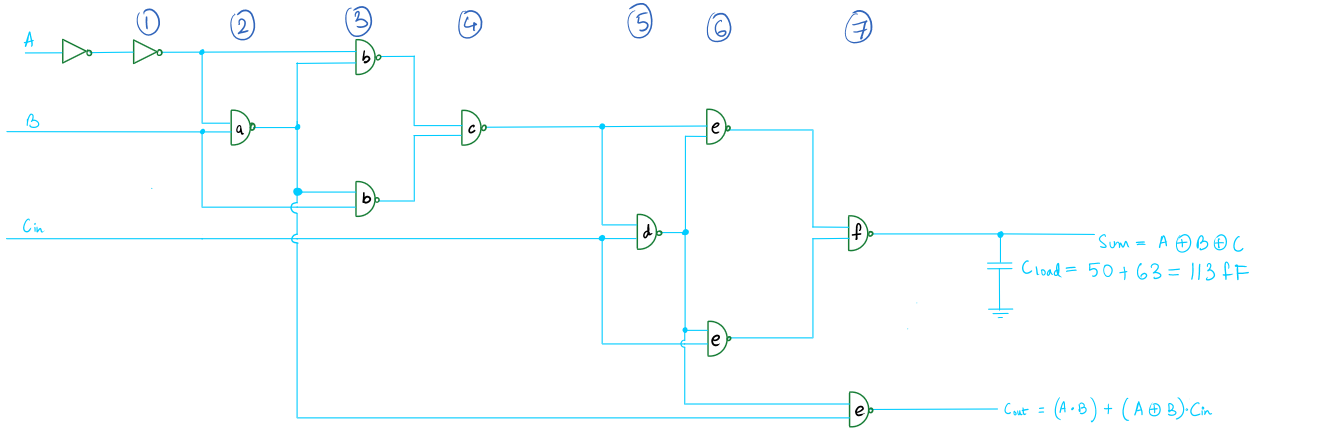
# **1. Pre-Lab**

## 1.1.



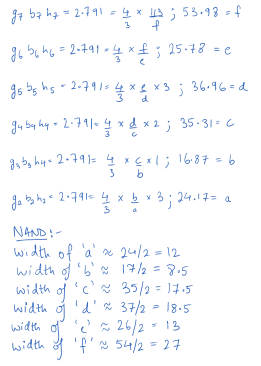
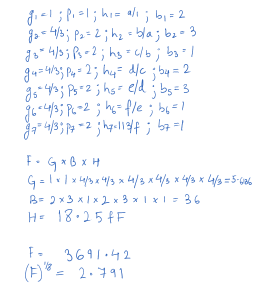
### *Figure 1: Truth table of a 1-bit full adder, and the Boolean logic derivation describing the S*

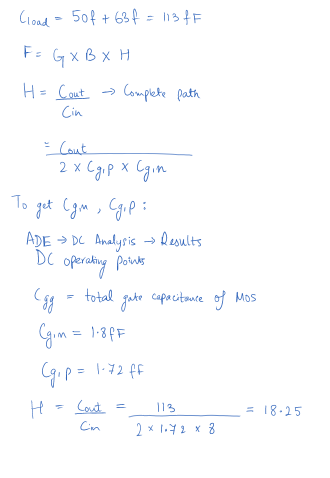
### *and Cout bits.*



### *Figure 2: Full Adder gate level schematic.*

## 1.2

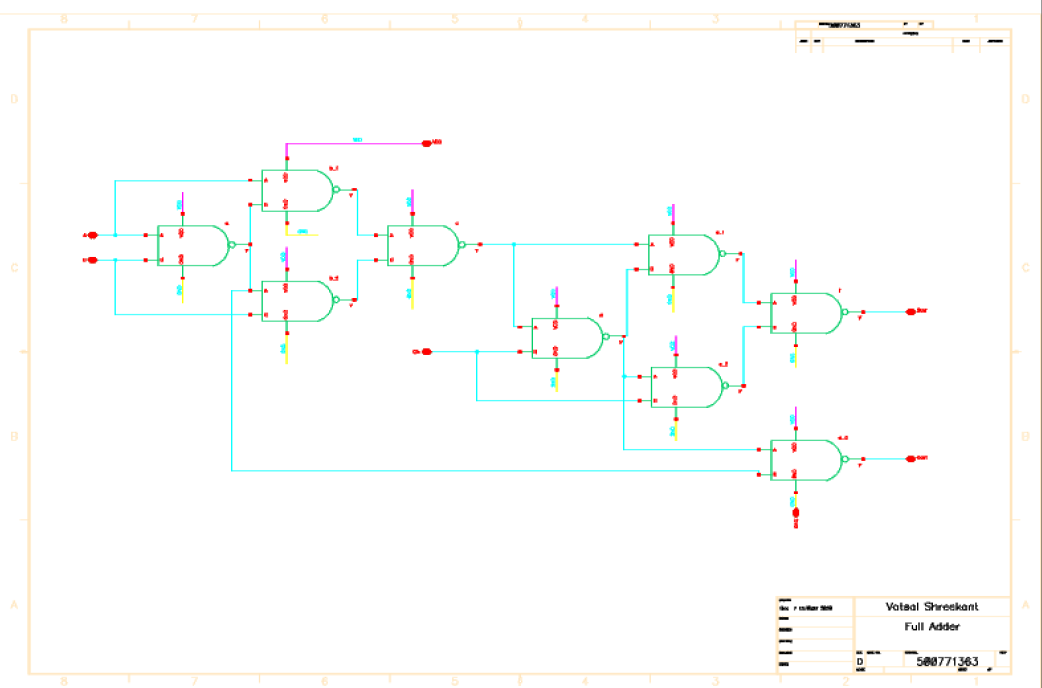




### *Figure 3: Full Adder sizing to drive a load capacitance of 113fF at the its sum output.*

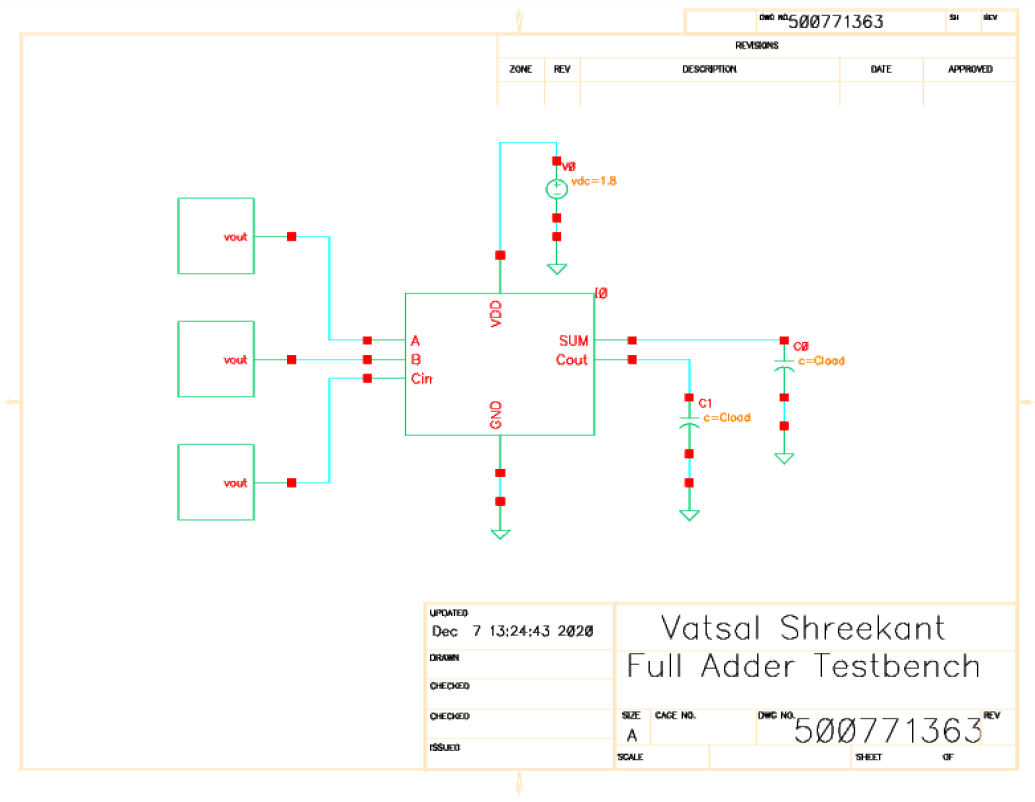
# **2. Post-Lab**

## 2.1 Schematic of Full Adder using NAND2 gates



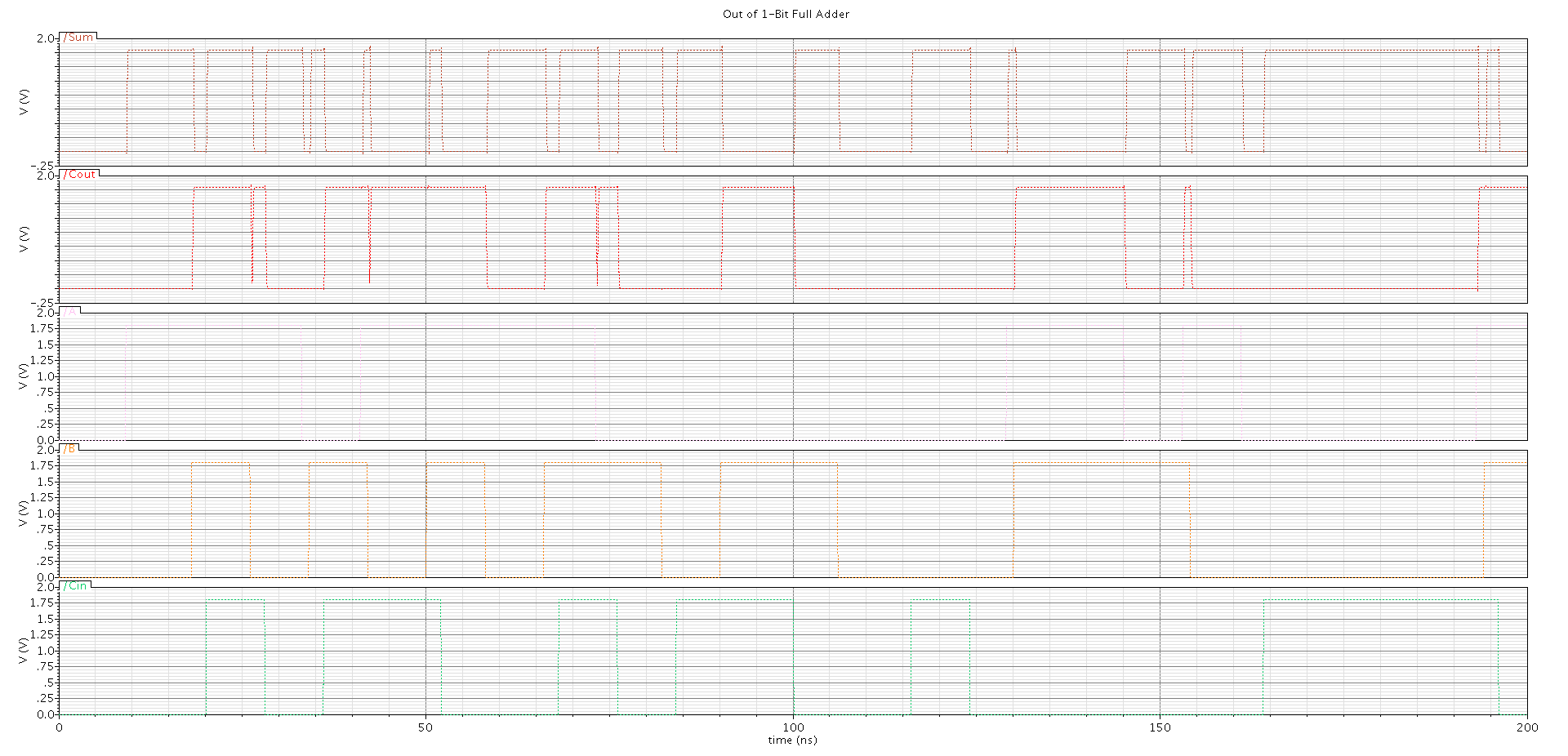
### *Figure 4:* *Schematic of 1-bit Full Adder*

## 2.2 Schematic of Testbench of Full Adder



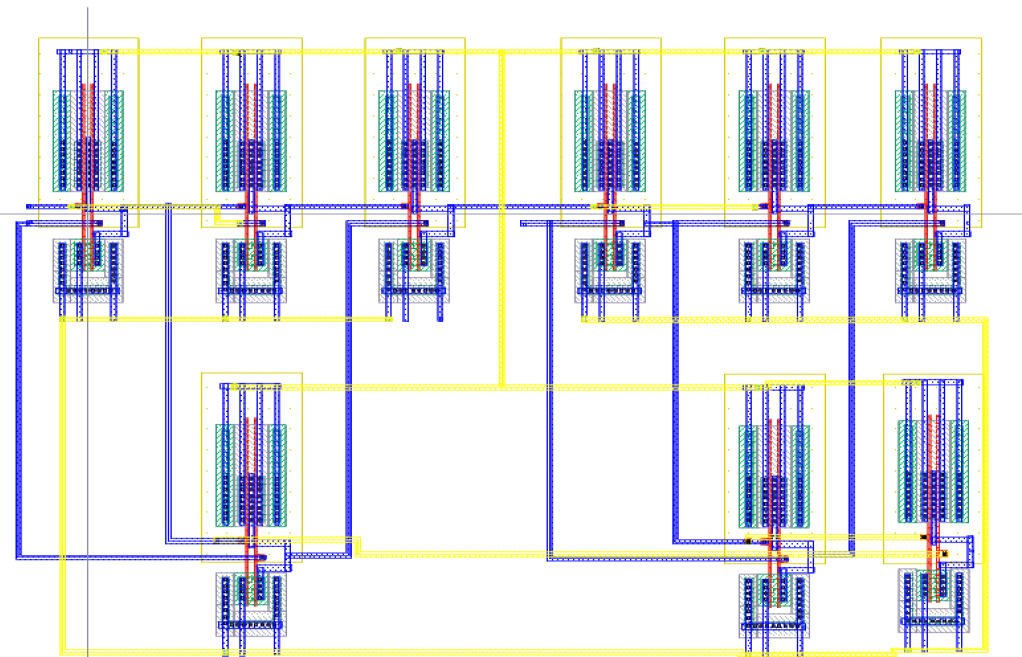
### *Figure 5: Schematic of Full Adder Testbench*

## 2.3 Simulation of full adder for 20ns to verify the functionality.

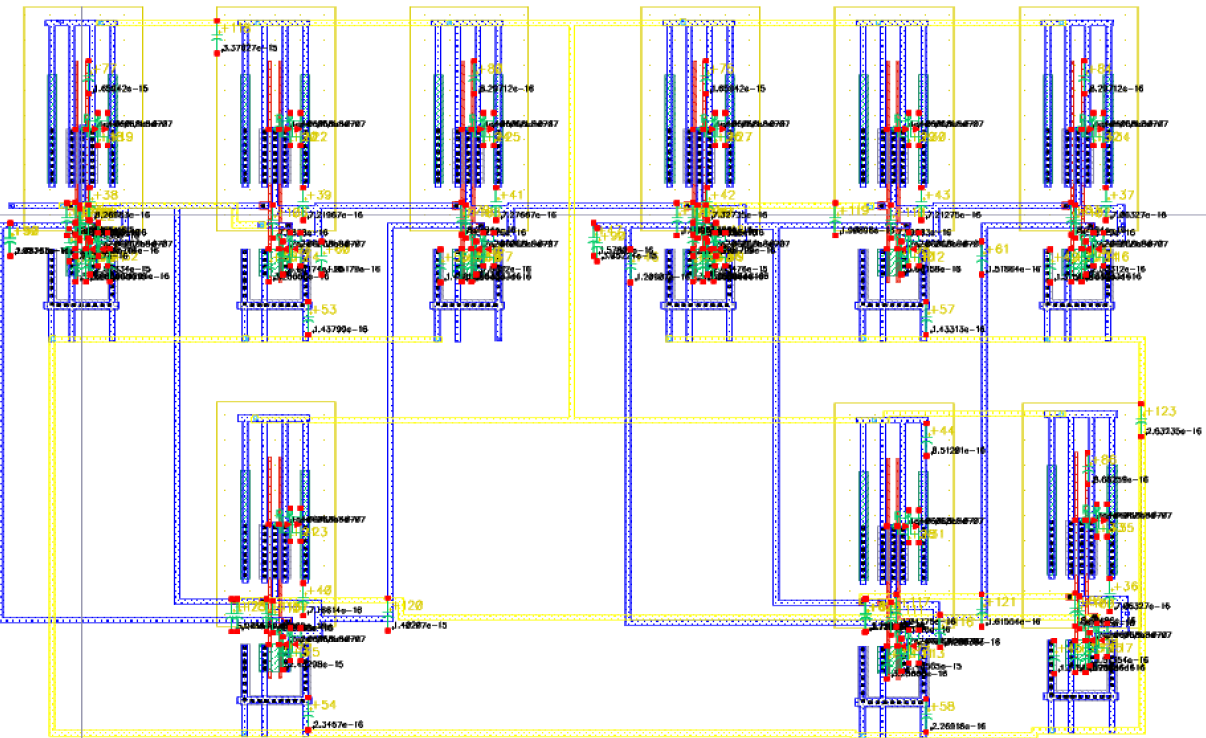


### *Figure 6: Simulation of full adder for 20ns*

## 2.4 Layout and Extracted Views of the Full Adder

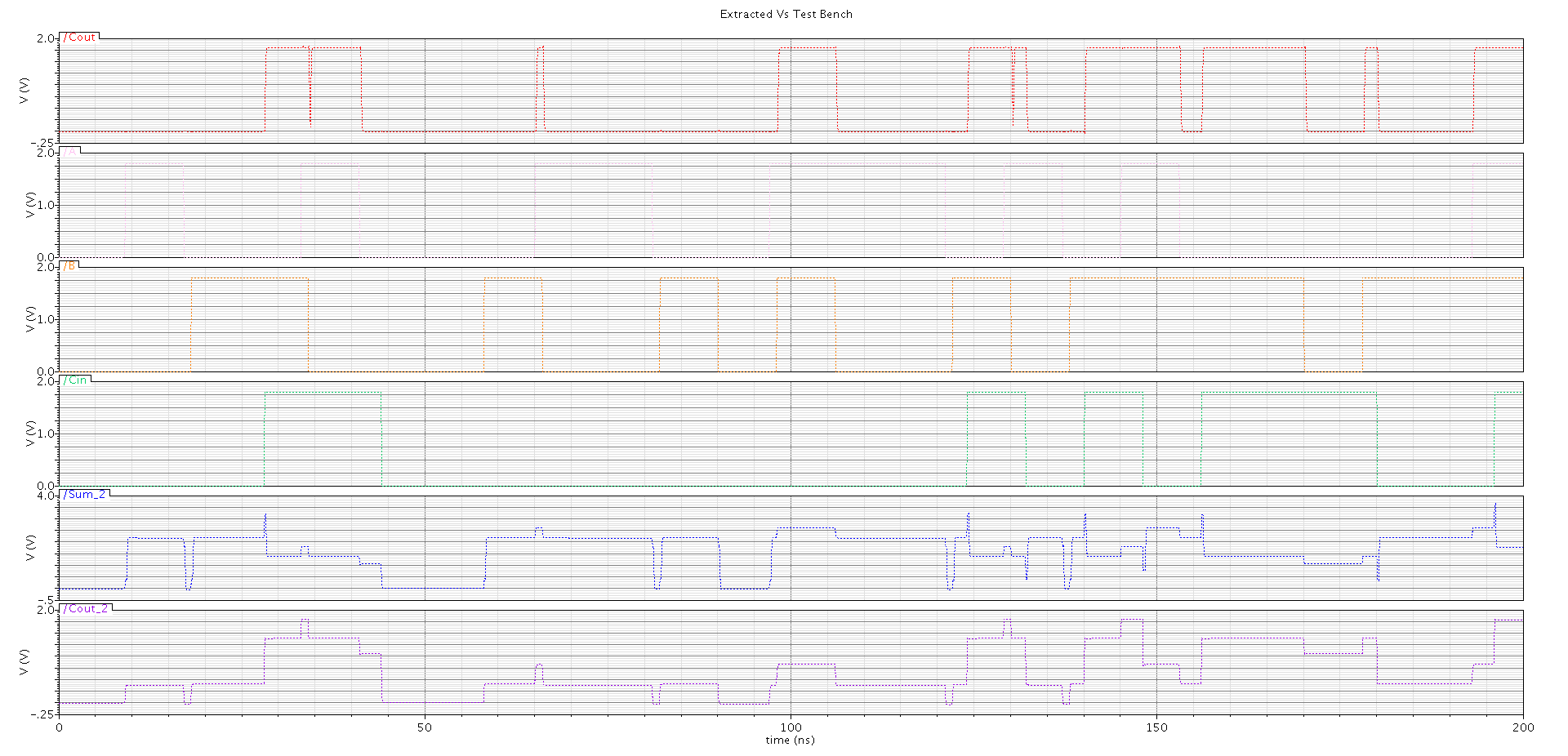


### *Figure 7: Layout View of Full Adder*

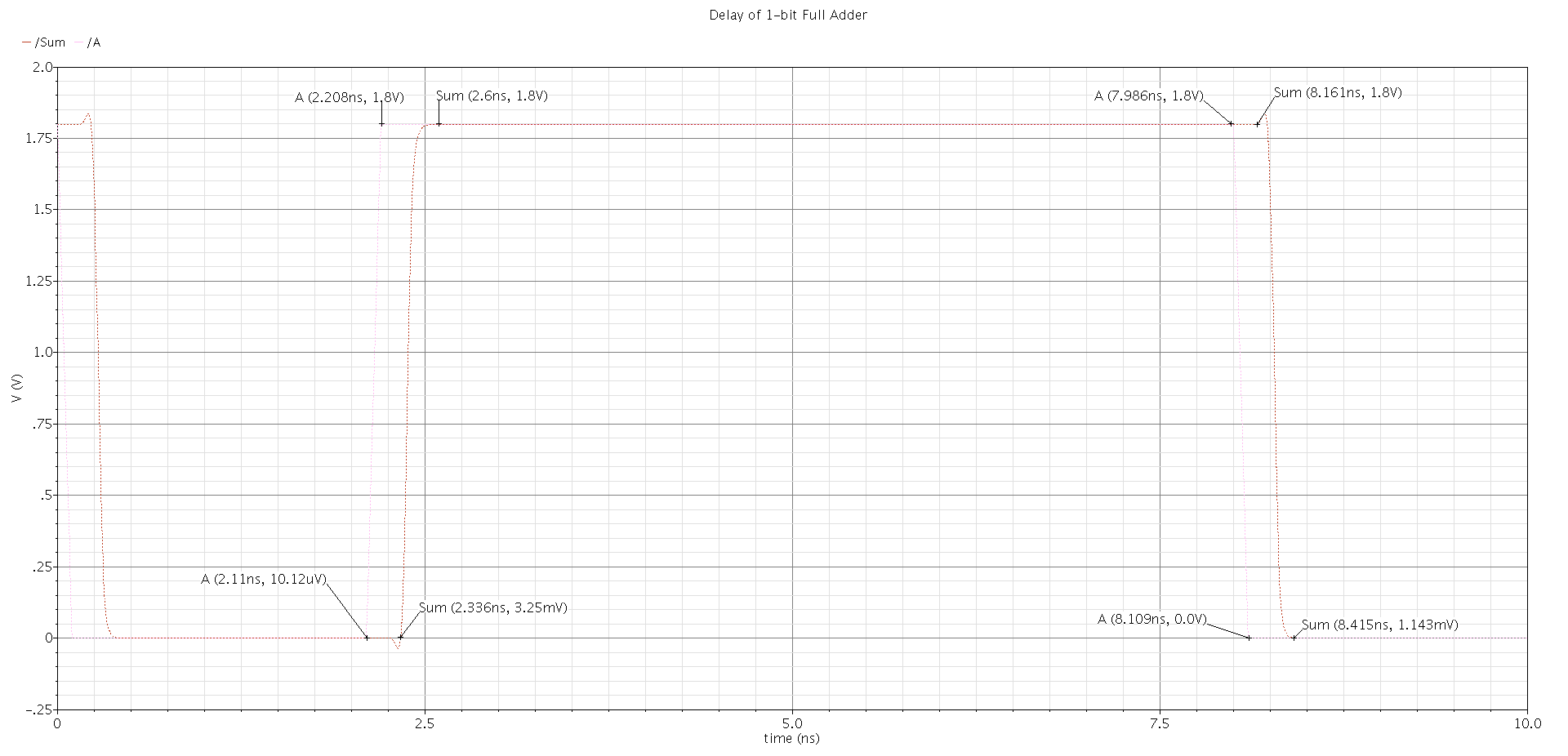


### *Figure 8: Extracted View of Full Adder*

## 2.5 Post-layout simulation.



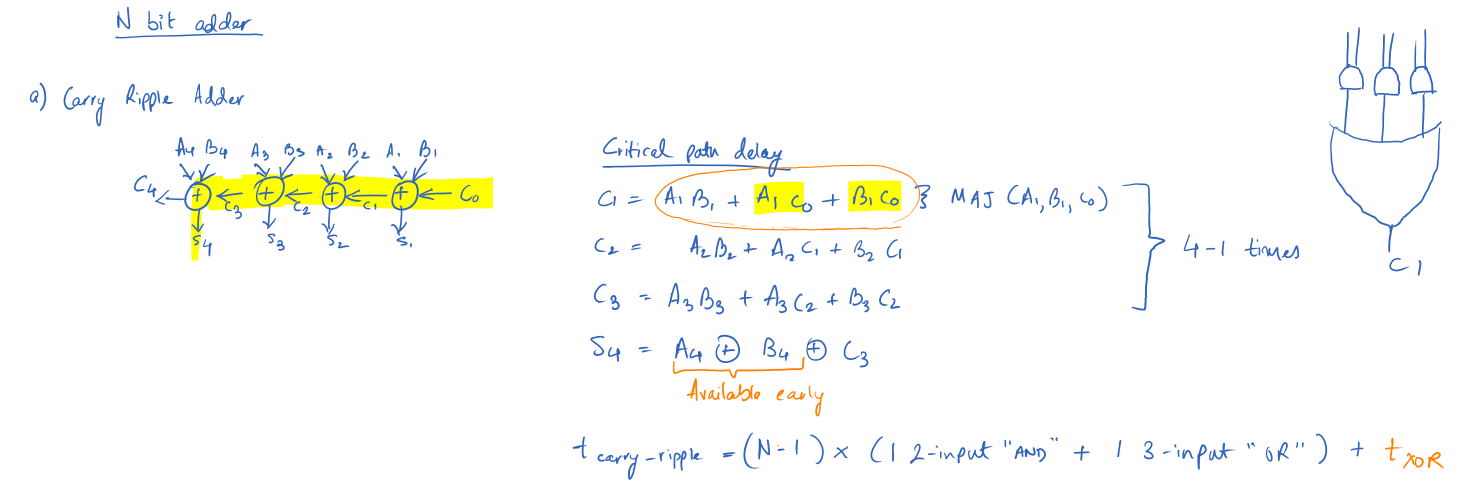
### *Figure 9: Results comparison of the extracted and testbench view.*



### *Figure 10: Simulation for vpulse inputs to measure the worst-case delay.*

## 3 Conclusion

This lab explored functionality of the Full Adder and its role as the building block for circuits meant for arithmetic operations. The simulations were performed through Transient and Parametric analysis. It was observed that the results obtained in the net list window were not perfect and had some discrepancies from the ideal simulation. The deviations between extracted and testbench view was very low for the worst-case delay. The delay was simulated with inputs of the full adder as ‘vpulse’. Moreover, in an instance when the worst case-delay for an ‘n-bit ripple carry adder’ arises, this can be then be attributed to the carry-in of the LSB propagates through to the MSB. The worst-case delay can be expressed as, tdelay as a function of the delay from tcarry (from Cin to Cout) and tsum (from Cin to Csum). Thus, it can be assumed that this lab was successful in execution.



### *Figure 11: tdelay expressed as a function of the delay from tcarry and tsum .*